

**CLAIM SET AS AMENDED**

1-4. (Canceled)

5. (Currently Amended) A method for manufacturing a semiconductor device comprising:

preparing a semiconductor substrate of a first conductivity type;  
forming scribe lanes **of the first conductivity type** in the semiconductor substrate, said scribe lanes defining chip formation areas and containing only an unetched portion of the semiconductor substrate;  
forming a deep well area in each chip formation area, each deep well area having a second conductivity type opposite the first conductivity type; and  
forming at least one well area within the deep well area.

6. (Previously Presented) The method of claim 5, further comprising forming a mask on the semiconductor substrate such that the deep well areas are formed in the chip formation areas and not in the scribe lanes.

7. (Previously Presented) The method of claim 5, wherein, the first conductivity type is a p-type conductor; and the second conductivity type is a n-type conductor.

8. (Currently Amended) A method for manufacturing a semiconductor device comprising:

preparing a semiconductor substrate of a first conductivity type;

forming scribe lanes of the first conductivity type in the semiconductor substrate, said scribe lanes defining chip formation areas;

forming a deep well area in each chip formation area, each deep well area having a second conductivity type opposite the first conductivity type; and

forming at least one well area within the deep well area,

wherein the first conductivity type is a n-type conductor; and the second conductivity type is a p-type conductor.

9. (Canceled)

10. (Currently Amended) A method for manufacturing a semiconductor device comprising:

preparing a semiconductor substrate of a first conductivity type;

forming scribe lanes of the first conductivity type in the semiconductor substrate, said scribe lanes defining chip formation areas and containing only an unetched portion of the semiconductor surface;

71 forming a deep well area in each chip formation area, each deep well area having a second conductivity type opposite the first conductivity type; and

wherein a first conductive well area and a second conductive well area are separately formed within the deep well area,

the first conductive well area is formed of the first conductivity type, and

the second conductive well area is formed of the second conductivity type.

11. (Previously Presented) The method of claim 5, wherein the scribe lanes are formed at all portions surrounding the chip formation areas.

12. (Previously Presented) The method of claim 6, further comprising removing the mask using plasma processing or plasma equipment.